

	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Inventor
1	US 20040247066 A1	20041209	50	Phase-locked loop circuit, delay locked loop circuit, timing generator, semiconductor test instrument, and semiconductor integrated circuit	375/376	327/156; 331/25	Suda, Masakatsu
2	US 20040213324 A1	20041028	18	High frequency spread spectrum clock generation	375/130	375/376	Hall, Paul Kevin et al.
3	US 20040028156 A1	20040212	16	System and method for performing on-chip synchronization of system signals utilizing off-chip harmonic signal	375/346	375/354	Sefidvash, Khorvish et al.
4	US 20030156662 A1	20030821	12	Device for the recovery of data from a received data signal	375/340	375/376	Engl, Bernhard et al.
5	US 20020181639 A1	20021205	9	Adaptive de-skew clock generation	375/373	375/354; 375/376	Song, Hongjiang
6	US 20020181633 A1	20021205	121	Means and method for a synchronous network communications system	375/354		Trans, Francois
7	US 20020141527 A1	20021003	12	Locked loop circuit	375/376		Song, Hongjiang
8	US 20020094055 A1	20020718	11	Unified digital architecture	375/376		Cranford, Hayden Clavie JR. et al.
9	US 20020067785 A1	20020606	38	High-speed transmission system having a low latency	375/354		Tanahashi, Toshio
10	US 20010033630 A1	20011025	20	Delay lock loop with clock phase shifter	375/376	327/158	Hassoun, Joseph H. et al.
11	US 20010033602 A1	20011025	25	Delay lock loop, receiver, and spectrum spreading communication system	375/140	375/376	Okubo, Seiji et al.

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12	US 6859107 B1	20050222	19	Frequency comparator with hysteresis between locked and unlocked conditions	331/11	327/43; 331/1A; 331/18; 331/DIG .2; 375/376	Moon; Yongsam et al.
13	US 6791420 B2	20040914	8	Phase locked loop for recovering a clock signal from a data signal	331/1A	327/156; 327/158; 327/159; 331/10; 331/25; 375/376	Unterricker; Reinhold
14	US 6788754 B1	20040907	10	Method and apparatus for de-skewing clock edges for systems with distributed clocks	375/375	327/158; 375/373; 713/401; 713/503	Liepe; Steven F
15	US 6775342 B1	20040810	53	Digital phase shifter	375/371	327/158; 327/161; 375/373; 375/376	Young; Steven P. et al.
16	US 6587534 B2	20030701	20	Delay lock loop with clock phase shifter	375/376	327/156; 327/158; 327/161	Hassoun; Joseph H. et al.
17	US 6522684 B2	20030218	24	Delay lock loop, receiver, and spectrum spreading communication system	375/147	375/141; 375/376	Okubo; Seiji et al.

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18	US 6396320 B2	20020528	65	Clock control method and circuit	327/156	375/376	Saeki; Takanori
19	US 6377640 B2	20020423	117	Means and method for a synchronous network communications system	375/354	370/286; 370/289	Trans; Francois
20	US 6292116 B1	20010918	17	Techniques and circuitry for accurately sampling high frequency data signals input to an integrated circuit	341/100	375/376	Wang; Bonnie I. et al.
21	US 6289068 B1	20010911	21	Delay lock loop with clock phase shifter	375/376	327/156; 327/158; 327/161	Hassoun; Joseph H. et al.
22	US 6262998 B1	20010717	6	Parallel data bus integrated clocking and control	370/503	375/354	Hogeboom; John Gordon
23	US 6144713 A	20001107	45	Delay locked loop circuit for controlling delay time with reduced lock-up time	375/375	327/161; 375/362; 375/376	Eto; Satoshi
24	US 6055287 A	20000425	8	Phase-comparator-less delay locked loop	375/376	327/156; 327/158	McEwan; Thomas E.
25	US 5939913 A	19990817	18	DLL circuit and semiconductor memory device using same	327/158	327/159; 327/236; 331/DIG .2; 375/376	Tomita; Hiroyoshi

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26	US 5777544 A	19980707	15	Apparatus and method for controlling data communications having combination of wide and narrow band frequency protocols	340/310.06	340/310.01; 340/310.04; 340/310.08; 370/344; 370/480; 375/222; 375/354	Vander Mey; James E. et al.
27	US 5428764 A	19950627	34	System for radial clock distribution and skew regulation for synchronous clocking of components of a computing system	713/503	307/409; 327/258; 327/292; 375/356; 714/700	Maskas; Barry A.
28	US 4095047 A	19780613	8	Phase regulating circuit	375/367	375/344; 375/376	von Pieverling; Klaus et al.